

ECE 563 Fall 2023 – Computer Architecture 1 for Graduate Students

Professor: Maria Striki

Syllabus

Instructor:

Name: Maria Striki

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Office: ECE 115

Teaching Assistant: TBA

Class Meets:

Time: Tuesday/Friday @ 8:30-9:50 am

Place: HLL-116

Final Exam: No Final – Main Project Presentations only

Computer Architecture Literature

Text book Official

D. A. Patterson and J. L. Hennessy, Computer Architecture: A quantitative approach, 6th Edition, Elsevier Publishing Co., 2017 (ISBN: 978-0-12-811905-1).

Additional Text Books:

D. A. Patterson and J. L. Hennessy, Computer Architecture: A quantitative approach, Fifth edition, Morgan Kaufmann Publishing Co., 2014.

D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 5th Edition, Morgan Kaufmann Publishing Co., 2014.

Random Reads:

Conference Papers, Journals, Research Problems and Projects provided in class.

ATTENTION: The official textbook can be purchased as ebook. However, you are going to be examined on material that is almost entirely based on PPT slides and examples I upload on CANVAS. So, you do not have to get this textbook right away, if you find you are familiar with the features of computer architecture covered during class.

Grading Guidelines

Grading (to be revisited beginning of October):

- Homework & Paper Reviews: ~15%
- Seminar Presentations and Reviews: ~10%
- Projects: ~10%
- Quizzes: ~15%
- Midterm Exam: ~25-30%
- Final Project and Presentation: ~20%
- Participation: X%
- NO FINAL EXAM ----

Homework:

Homework to be handed at the beginning of the class. Some are individual and some will be group work.

Quizzes:

No make-up exams except for university sanctioned reasons.

Midterm will be held between mid October and beginning of November.

Project and Class Presentations:

To be conducted in groups of 1-2 students (or 3 depending on the final size of the class – TBA at the end of week 2).

It is not implied that group members get the same grade. Your grade will be based on your individual effort and on how your presentation/participation/presence is perceived by the professor and your reviewers each time you present.

Class Layout:

This class will be a combination of lectures on selected topics of Computer Architecture and a number of presentations and reviews by/from students on selected topics (either of their own choice or proposed by students themselves).

Required Background

--- **Basic Computer Architecture and in particular RISC-V and/or MIPS architecture.** There will be few introductory lectures on RISC-V just as refreshers. Please do not take the class if you do not have any previous familiarity with this type of assemblers.

--- Familiarity with how to write, compile and run programs in a higher level language (C, C++, Java).

--- Familiarity with how to represent and operate on positive and negative numbers in binary form.

--- Basic familiarity with logic design is encouraged but not necessary (Boolean algebra, logic minimization, decoders and multiplexors, latches and flip-flops, registers, finite state machines, etc.).

Course Outline

- Introduction
- Fundamentals of quantitative design and analysis
- Pipelining & Pipeline hazards (Data Hazards, Control Hazards, Resource Hazards)
- Instruction Level Parallelism (Out-Of-Order execution, Tomasulo Algorithm, Re-order Buffer, Branch Prediction)
- VLIW and Multi-scalar
- Memory hierarchy
- Multiprocessors
- Multithreading
- Your own suggestions and choice on topics of interest!
- And perhaps more topics not necessarily in the order mentioned above.

Course Goals

Ability to design pipeline architectures and to optimize them with respect to different constraints: size (cost), speed, power dissipation, and reliability.

- Discussing major architectural design patterns, including pipelining, in-order and out-of-order superscalars, SIMD, etc.
- Discussing memory design and hierarchies
- Discussing Parallelism