

Fall 2023

VLSI Design

Course number 14:332:479 / 16:332:574

Time and location: Mondays and Wednesdays from 5:40 - 7 pm in BE 213 on Livingston campus

Instructor: Taerin Chung, Ph.D.

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Office hour/location: TBA

Course overview/description

This course introduces the fabrication and layout techniques necessary to design Very Large Scale Integrated circuit (VLSI) systems. Specific topics include: CMOS digital logic, fabrication process technology, MOSFET theory, layout design rules including all the factors required for an effective circuit design, and case study of IC chips and microprocessors.

Topics covered

- 1) Introduction of VLSI systems
- 2) Physical Design of IC chip
- 3) CMOS circuit and logic
- 4) Basic CMOS fabrication process
- 5) MOS Transistor theory
- 6) CMOS Processing technology
 - layout Cells and Stick Figures/ Design rules
- 7) Delay
- 8) Logical Effort
- 9) Power and design for low power
- 10) Circuit simulation
- 11) Interconnects in CMOS technology
- 12) Memory (SRAM, Flash memory, etc.) design
- 13) Design methodology and tools
- 14) Nanoscale design issues
- 15) Testing and Introduction to Verilog

Course objective

A student is expected to be able to design basic digital CMOS circuits, estimate and predict key system characteristics such as area, speed, and power depending on technology, and understand various design methodologies (such as custom, semi-custom, standard cell, and gate array) that incorporate such circuits into bigger digital systems.

- Understand how modern silicon technology enables the implementation of digital circuits on a single chip.
- Understand the relationship between the transistor fabrication parameters and their effects on key parameters of digital systems such as area, power, and clock rate.

Reference textbook

CMOS VLSI Design by Weste and Harris, 4th edition, Addison-Wesley/Pearson, 2011
In addition, handouts developed by instructor may be downloaded

Grading

Homeworks/Project with SPICE simulation: 35%

Mid-term exam (open-note) : 25%

Final exam: 30%

Review paper:20%

* Extra credit for the layout work using the Layout Editor