Electrical and Computer Engineering, Rutgers University
Spring 2024
Deep Sub-Micron VLSI Design

Course number 16:332:578:01

Time and location: Mondays and Thursdays, 8:30 AM – 9:50 AM, in SEC-216

Instructor: Taerin Chung, Ph.D.

Email: taerin.chung@rutgers.edu

Course overview/description

As a continuation of VLSI design, combinational, sequential circuits, and data path subsystems for VLSI design are introduced. By aiming to a single-nanoscale VLSI Chip, this course focuses on the design methodologies on each level including logic design, circuit design, and physical design (floorplanning), emphasizing low-power/low voltage, cost-effective strategy. To overcome Deep Sub-Micron scaling issues, nanoscale-VLSI technologies are addressed and reviewed, underlining the novelty and feasibility with concurrent VLSI/ULSI technologies.

Topics covered

- Review of VLSI Design, Standard Cell
- Combinational logic circuits
- Circuit Pitfalls (SOI/Subthreshold Circuit design)
- Process variation and Automated design
- Design methodology and Economics
- Programmable logic
- Arithmetic building block
- Datapath subsystem: Addition/Subtraction (*i.e*. Full adder)
- Dynamic logic/Memory
- Low Power design techniques for VLSI chips
- Nanoscale VLSI:
  1) Chip-level Optical Interconnect
  2) Register-Transfer-Level Design for Application-specific Integrated Circuits
  3) Emerging Graphene FETs for Next-generation Integrated Circuit Design (GFET-based inverter)

Reference textbook

CMOS VLSI Design by Weste and Harris, 4th edition, Addison-Wesley/Pearson, 2011

Nanoscale VLSI: Devices, Circuits and Applications, Rohit Dhiman, Rajeevan Chandel, Springer 2020

Handouts and reference articles developed by instructor will be downloaded.

Grading policy
Above 75% attendance is required.

1) Homeworks (total 3):
   2 HWs - Practice problems/research: 30%
   1 HW - Design + simulation by cadence virtuoso/LtSpice/layout editor):25%

2) Performance of problem-solving project (Teamwork in Class, one-time): 15%
3) Final exam (open-book, take-home exam): 30%

Note: Students are expected to attend all scheduled sessions of the courses for which they are registered.

Note: Late submission of all assignments will carry a penalty of 10% per day with a maximum penalty of 50%. Extensions will NOT be allowed without prior permission from the instructor.