ECE 578 – Deep Submicron VLSI Design

This course provides a comprehensive overview of deep submicron (DSM) VLSI design, bridging foundational knowledge with emerging technologies. Students will begin with a brief review of Digital Logic Design (DLD) and Verilog-AMS coding, semiconductor structures and characteristic functions, establishing the basis for advanced topics including DSM design challenges, floor planning, power planning, thermal dissipation, clock tree synthesis, data routing, and 3D integrated circuit (IC) design.
To complement technical content with real-world innovation, the course incorporates the use of USPTO Public Patent Search tools to explore recent advancements in DSM technologies. The course concludes with a comparative study of CPU vs. GPU architectures and an introduction to SystemVerilog for modern hardware design.

Class Syllabus:

Week 1: Semiconductor manufacturing process; advantages/issues/solutions of DSM; introduction to USPTO public patent search tools; Google patent search; Verilog vs VHDL; hardware vs software development; advantages of abstract design; HDL-based ASIC design flow

Week 2: Digital Logic Design review; Verilog coding/testbench review; Finite State Machine revies; synthesizable RTL code; Advanced RISC Machine; Verilog Primitives, Verilog Strengths Qualifiers, Verilog net types and user defined primitives, Verilog build a capacitor

Week 3: Diode, BJT, MOSFET, and their characteristics functions; doping, n/p MOS transistor physical structure, operation, characteristic function, logic properties, pull up/down circuits, S/D doping reduction effects, halo implant in DSM, DSM band-to-band tunneling, electromigration.

Week 4: Verilog modeling propagation, rise, fall, turn-off delays, nested module, event-driven simulation and testbench structure. Photolithograph: process flow, critical dimension, alignment in nanometer, photoresist, optical proximity correction, source mask optimization, photolithograph aberration; resolution enhancement methodologies.

Week 5: Demonstrate the emerging DSM technologies from patent search, e.g., Gate-Overlapped LDD (lightly doped drain), halo implant in semiconductor structure; patent US 7,393,752 B2 Semiconductor Devices and Method of Fabrication; US patent 6,949,796 B1 Hallo Implant In Semiconductor Structures.

Week 6: DSM halo implant trade-offs; US 7,192,836 B1 Method And System For Providing Halo Implant To A Semiconductor Device With Minimal Impact To The Junction Capacitance; US 10,778,092 B2 Negative Voltage Generating Circuit Having Automatic Voltage Adjustment Function; EUV (Extreme Ultraviolet Radiation) optics; floorplan overview; cell library and testbench, inertial/transport delay

Week 7: Floorplanning: design partitioning, aspect ratio, size & area utilization, macro placement, pin placement, power routing, global signal planning, signal integrity, thermal considerations, design for manufacturability, design rule checks.

Week 8: Power routing/planning: voltage scaling challenges, on-chip voltage regulators (switching regulators, low-dropout regulators), multiple voltage domains, power gating and sleep transistors (header/footer switching cells, fine-grain/coarse-grain power gating, isolation cells, state retention & retention registers), particle swarm optimization (on-chip/off-chip power shut-off), power integrity and noise management, voltage islands, dynamic voltage and frequency scaling (DVFS), leakage power management (reverse body biasing, adaptive body biasing), thermal management

Week 9: Power grid topologies, levels of power distribution, power island; power grid design (types of metal layers), dynamic power management; inputs/outputs of VLSI power supply design; simulation and validation; overview of 3D IC and advanced packaging.

Week 10: Thermal Dissipation: electrical energy & heat energy, fundamental laws electromagnetism, Eddy currents, thermal conductivity (Fourier's law), heat balance equation, electrothermal electrical analogy (heat generation/cumulation/transfer), thermal conductor materials (in ICs and packaging), thermal interface materials, 3D IC thermal collection, thermal collection network, heat dissipation challenges/design strategies (device level, material level, packaging level, simulation modeling)

Week 11: DSM clock tree synthesis (CTS): goals/challenges, buffered clock tree, CTS design inputs, clock latency/skew/slew/jitter, clock delivery (minimum pulse width, duty

cycle check, clock power/gating, use of multi-bit registers), minimum clock period calculation, clock duty cycle distortion, minimizing clock skew, phase-locked loop (PLL), clock tree architectures (single point CTS, clock mesh, multi-source CTS, H-tree, X-tree, geometric matching algorithm, pi-tree, fish-bone structure), crosstalk noise on the clock network, non-default routing (NDR) rules, design steps in CTS (Cadence EDA flow), CTS exceptions (stop pin, nonstop pin, float pin, exclude pin), clock tree optimization, CTS design outputs, check after CTS.

Week 12: DSM data routing: data routing challenges, data routing delay, interconnection modeling, source of the parasitics, the parasitics extraction (resistance/capacitance/inductance extraction), routing steps

Week 13: TSMC 3DFabric®: IC packaging (wafter/panel fan-in/fan-out, TSMC InFO), 2.5D packing (WoW vs CoW, CoWoS-S/R/L), 3D packaging (front-end 3D, back-end 3D, SoIC), cost/performance improvements through chiplets integration, AMD Instinct MI300 – AI+HPC

Week 14: CPU vs GPU: CPU architecture bottlenecks (power wall, memory wall, ILP wall), CPU vs GPU design philosophy, GPU for general-purpose computing, Nvidia GPU architecture (GeForce 7800, GeForce 8800, Fermi SM), Nvidia GPU programming model (CUDA instruction set). SystemVerilog: base class, child (derived) class, constructor, virtual function/task, pure virtual function/task, abstract class, polymorphism.